VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) An apparatus comprising:

a first circuit configured to present a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals; and

a second circuit configured to present said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

9. (AMENDED) A circuit comprising:

means for generating a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals; and

means for generating said one or more serial data signals and said first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

10. (AMENDED) A method for controlling a pulse width in a phase and/or frequency detector comprising the steps of:

(A) generating a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals; and

(B) generating said one or more serial data signals and said first clock signal in response to (i) a second clock signal

and (ii) a parallel input data signal, wherein said first clock signal is configured to control said pulse width.

17. (NEW) The apparatus according to claim 1, wherein said second circuit is configured to generate a plurality of said serial data signals.

18. (NEW) The apparatus according to claim 1, wherein said first circuit is configured to receive to a plurality of serial data signals.

19. (NEW) The apparatus according to claim 9, wherein said second circuit is configured to generate a plurality of said serial data signals.

20. (NEW) The apparatus according to claim 10, wherein said second circuit is configured to generate a plurality of said serial data signals.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus comprising a first circuit and a second circuit. The first circuit may be configured to present a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals. The second circuit may be configured to present the one or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal.

IN THE DRAWINGS

While Applicant's representative does not necessarily agree with the requirement to label FIG. 1, in order to further prosecution, FIG. 1 has been labeled "conventional". As such, the objection to the drawings should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-16 under 35 U.S.C. §102 as being anticipated by Mullaney et al. '575 is respectfully traversed and should be withdrawn.

Mullaney discloses a high speed cross point switch routing circuit with a word-synchronous serial back plane (Title).

In contrast, the present invention provides a first circuit configured to present a parallel output data signal in response to (i) a first clock signal and (ii) one or more serial data signals. A second circuit may be configured to present the one or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal. It is unclear how the so-called second circuit (element 62 of FIG. 5b of Mullaney) presents both one or more serial data signals and the first clock signal as presently claimed. In particular, the so-called first clock signal (BCLK in FIG. 5 of Mullaney) is not presented from circuit 62, but rather from the element 58. The line in the drawing from the element 58 (of FIG. 5b of Mullaney) crosses the output of the element 62 in FIG. 5b of Mullaney. This crossing is notated by the lack of a node. A generally accepted symbol used to show a connection in an electrical circuit diagram. A crossover indication is clearly shown. Applicants' representative believes this may have been an oversight by the Examiner. If another interpretation was intended, clarification is requested.

Furthermore, the so-called first circuit (element 60 in FIG. 5 of Mullaney) does not appear to receive a clock signal (the signal BCLK), as presently claimed. In particular, the signal BCLK is presented to the element 98. Additionally, the so-called second circuit (element 62 of Mullaney) does not appear to respond to a

second clock signal (the signal WCLK), as asserted by the Examiner. The claimed second circuit responds to (i) a second clock signal and (ii) a parallel input data signal. Mullaney does not disclose or suggest each of the elements of the present claims. As such, the presently pending claims are fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, newly presented claims 17 and 18 provide that the first circuit response to a plurality of serial data signals. The so-called first circuit (element 60 of Mullaney) only responds to a single serial data signal. The so-called second circuit (element 62 of Mullaney) presents, at best, only a single serial data signal. Neither the first signal nor the second signal of FIG. 5 of Mullaney respond to a plurality of serial data signals as in the newly presented claims 17 and 18. As such, claims 17 and 18 are independently patentable over the cited reference and the rejection should be withdrawn.

In conclusion, Mullaney does not disclose or suggest a second circuit configured to present the one or more serial data signals and the first clock signal in response to (i) a second clock signal and (ii) a parallel input data signal. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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